REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-7 remain in the application. Claims 1-7 are under prosecution. Claim 8 has been canceled.

In items 2 and 3 on pages 2-4 of the above-identified Office Action, claims 1-7 have been rejected as being anticipated by Nakada (US Pat. 5,148,396) under 35 U.S.C. § 102 (b).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Nakada teaches a memory circuit having a memory cell array S1 containing a plurality of memory cells. The memory cell array S1 includes a plurality of word lines and a plurality of bit lines for addressing the plurality of memory cell. The memory cells are disposed at cross-over points of the word lines and the bit lines. A plurality of write amplifiers 101-104 are provided for writing to the plurality of memory cells. Each of the write amplifiers is assigned to a group of bit lines. An address decoding circuit is provided for simultaneously

activating a group of the write amplifiers, depending on a test signal so that the group of the write amplifiers writes test data to the group of the memory cells via respectively assigned ones of the bit lines. However, Nakada does not teach using a part of an address of the bit lines to be responsible for selection of a y-segment of the memory cell array.

In contrast thereto, Nakada describes the masking of write data input by respective write mask data input circuits, which do not receive any address values. The address values in Nakada are referenced by A1, A2, A and are applied to the selector 70 and the write mask decoder 90 to channel the masked write data to the column address decoder S3 such that the mask write data is applied to the memory cell at a memory address given by the address values A1, A2. However, a masking of the address such that more than one write amplifier is activated due to the masked part of the address is not disclosed. It is merely provided that a four-bit-configuration has a special mode, wherein the control signal for all of the write amplifiers go high, thereby activating all of the write amplifiers. It is not disclosed that this is performed by masking the address signals A1 and A2.

More specifically, claims 1, 4 and 7 of the instant

application recite "masking a part of an address of the bit lines which is responsible for selection of a y-segment of the memory cell array". Consequently, it is believed that claims 1, 4 and 7 of the instant application are not anticipated by Nakada as Nakada does not teach this feature.

In item 4 on pages 4-5 of the above-identified Office Action, claims 8 has been rejected as being anticipated by Hatakeyama (US Pat. 6,337,820) under 35 U.S.C. § 102 (b).

Claim 8 has been canceled and therefore the rejection is now moot.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1, 4, or 7. Claim 1, 4, and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 4.

In view of the foregoing, reconsideration and allowance of claims 1-7 are solicited.

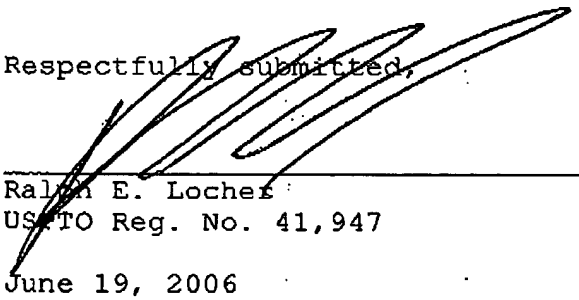
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer, LLP., No. 12-1099.

Respectfully submitted,



Ralph E. Locher
USPTO Reg. No. 41,947

June 19, 2006

Lerner Greenberg Stemer, LLP.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101